

## The PICNIC Interferometry Camera at IOTA

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**ABSTRACT.** We describe the control and performance of a new near-infrared camera based on a Rockwell PICNIC array detector for interferometry observations at the Infrared-Optical Telescope Array (IOTA). The camera control uses a complex programmable logic device that allows fast and stable clocking of the PICNIC array and on-the-fly reconfiguration of the readout method. We measured a read noise as low as 12.4  $e$  per correlated double sample. The read noise can be reduced even more through nondestructive readout, and decreases as the square root of the number of successive reads. We discuss the advantages of this system for near-infrared interferometry.

### 1. INTRODUCTION

IOTA is a long-baseline optical interferometer located at the Smithsonian Institution Whipple Observatory on Mount Hopkins, Arizona, comprising three 45 cm telescopes that can be positioned at 17 stations on an L-shaped track, the arms of which are 15 m toward the southeast and 35 m toward the northeast. IOTA operated with two telescopes from 1995–2003, and three telescopes since 2002 February. The interferometer is described in Traub et al. (2000, 2003), recent technical results are in Berger et al. (2001) and Monnier et al. (2003a), and recent science results are in Kervella et al. (2001), Mennesson et al. (2002), Chagnon et al. (2002), Hofmann et al. (2002), Monnier et al. (2003b), Ohnaka et al. (2003), Millan-Gabet et al. (2003), and Weigelt et al. (2003).

In parallel with the upgrade from two to three telescopes, we also upgraded from distributed computers to a uniform platform based on the real-time operating system VxWorks running on three Power-PC single-board computers. Our final major upgrade was from a NICMOS3 camera (Millan-Gabet 1999; Millan-Gabet et al. 1999) to a PICNIC detector system. The camera controller uses a complex programmable logic device (CPLD), ca-

pable of fast and stable clocking of the array typical of hardwired digital circuits. The use of a CPLD allows on-the-fly reconfiguration of the readout method that was implemented through less stable infrared/optical (I/O) software in our previous NICMOS3 camera. CPLDs achieve the same clock stability of hardwired logic. Other groups have obtained comparable results using transputers-based controllers (McLean et al. 1993, 1994; Probst et al. 1994; Joven-Alvarez et al. 1994), bit-slice processors (Chin & Gezari 1987), digital signal processor-based controllers (Fischer et al. 2003), and combination of these technologies. This paper describes the new detector system and its performance with the three telescope interferometer.

### 2. OVERVIEW OF THE PICNIC SYSTEM

The PICNIC detector array (Kozlowski et al. 2000; Cabelli et al. 2000) is a  $256 \times 256$  pixel HgCdTe array arranged in four quadrants of  $128 \times 128$   $40 \mu\text{m}$  pixels and sensitive to the 0.8–2.5  $\mu\text{m}$  wavelength region. It is an improved version of the NICMOS3 detector; both are made by Rockwell Scientific. We upgraded from NICMOS3 to PICNIC with the expectation that the new detector would have lower intrinsic read noise.

Mechanically, the new liquid-nitrogen dewar is an improved version of the previous one, with two motorized filter wheels in place of a hand-rotated single filter wheel. Electronically, the analog and digital circuitry is also a copy of the previous camera, with the exception of the camera controller (described in the Appendix), which is CPLD-based and replaces the PC used in the previous system. This important upgrade was undertaken with the expectation that hardware-based clocking would be faster and more stable (Murphy et al. 1995). The on-the-fly reconfigurability of the clocking patterns (readout

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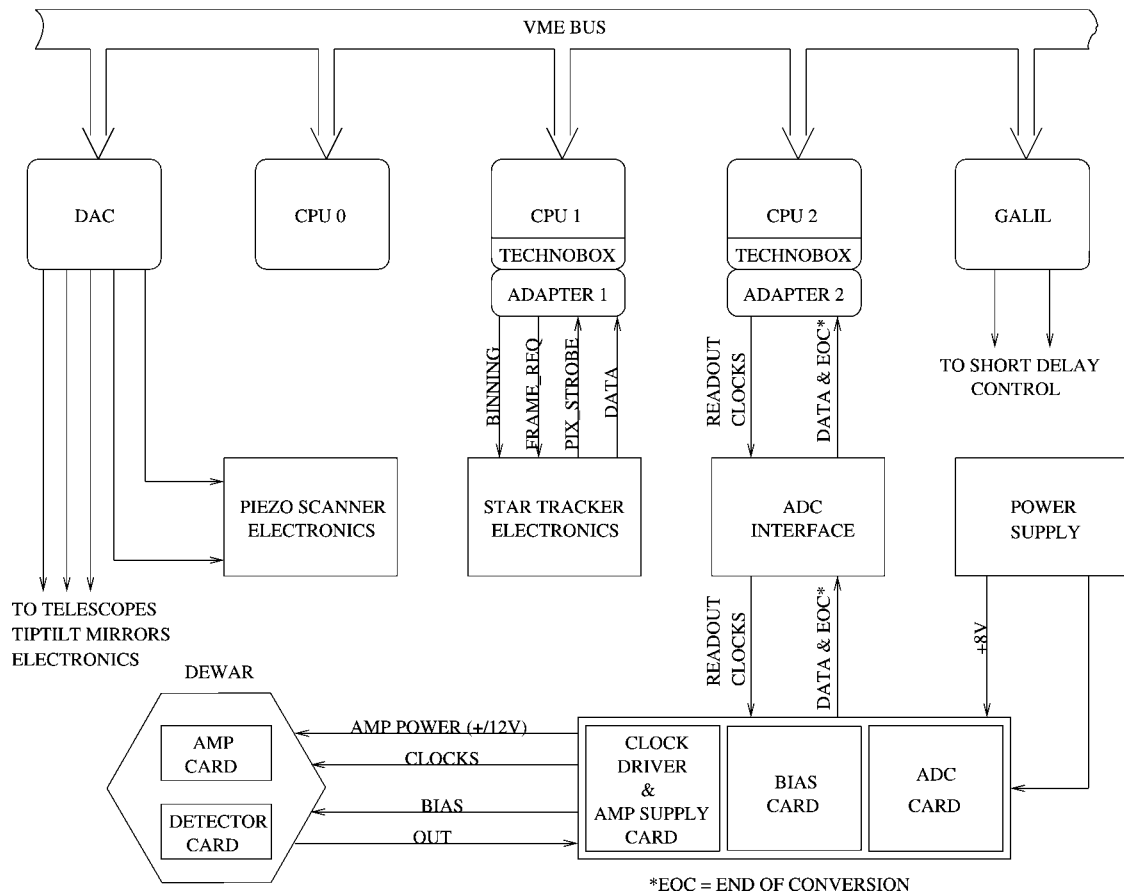


FIG. 1.—Control system block diagram at IOTA. The three CPUs (or single-board computers) manage different functions of the IOTA interferometer. CPU-2 is dedicated to data acquisition and fringe tracking. The CPLD on the Technobox interface performs all the tasks necessary to the PICNIC camera operation.

modes) afforded by CPLDs is a highly desirable property under conditions of experimentation. A test-bed interferometer like IOTA in fact uses various schemes of optical beam combination that need reconfigurable readout modes. A block diagram of the system is shown in Figure 1.

The overall improvements to the system are: (1) PICNIC has a line-by-line reset instead of a pixel-by-pixel reset. The expected advantage is to reduce noise from pixel resets (reset anomaly) and a faster reset cycle. (2) The line and pixel clocks (see § 3.4) are single-edged in NICMOS3 but double-edged in PICNIC. The advantage is a factor of 2 gain in clocking speed. (3) The output source follower in PICNIC can be turned off when not in use. The expected advantage is a decrease in spurious signal from source follower glow. (4) The user-controlled CPLD clock cycle is very stable, whereas a PC-generated clock might suffer delays if a background process is operating. The advantage is a very constant effective integration time from sample to sample. This effect has long been apparent to workers in this field interested in photometric accuracy and general system robustness (Murphy et al. 1995). (5) Faster clocking in PICNIC indirectly gives a lower effective noise, because we can read each pixel more often within a given integration time and thus further average down the read noise. (6) Unloading the timing, data acquisition, and

basic data processing from a computer CPU to a CPLD means that the CPU has more time to spend on other tasks, such as active fringe tracking. (7) The CPLD can be easily switched from one interferometric readout mode to another. For example, a full- or partial-frame readout might be used to align several star images within specific target pixels, after which the handful of target pixels can be repeatedly read out in any desired time sequence. (8) The same CPLD card type is used for the PICNIC camera, the visible star tracker, and the advance photodiode detectors (APDs) used for the visible beam. The advantage is in using the same software drivers and routines all over again and in maintaining fewer spare parts by using the same card. (9) The circuit of the CPLD camera controller could be implemented separately from the VME computer backbone with minor hardware modifications.

### 3. CAMERA ELECTRONICS

#### 3.1. Analog Electronics

The analog electronics of our new PICNIC camera are identical to the electronics used in the IOTA NICMOS3 camera (Millan-Gabet 1999; Millan-Gabet et al. 1999). However, the printed circuit board (PCB) on which the detector itself is

mounted is different, since the PICNIC and NICMOS3 carriers are not pin-to-pin compatible.

### 3.2. Noise Reduction

To minimize read noise, it is important to practice defensive tactics in implementing the circuitry. We used the following techniques: (1) The camera analog electronics are decoupled from the outside world by using opto-isolators on all digital signals. (2) The PCBs are carefully designed to separate the local digital ground of the opto-isolators from the analog ground. (3) Separate digital and analog ground planes were laid out around digital and analog components in order to shield out interference from the switching of the opto-isolators and other digital circuits. (4) Both grounds are connected to the metal chassis at a single point to avoid ground loops. (5) All the interconnection cables to and from the dewar are shielded to avoid electromagnetic interference. (6) Switching power supplies elsewhere in the lab were replaced with non-switching ones. The advantage was noticeable. (7) Externally generated high-frequency noise at the 110 V ground wire initially appeared on our analog data line, adding a few electrons of noise, but was eliminated by grounding the camera electronics through a choke wound around a ferrite core.

### 3.3. CPLD Technology

A CPLD, and its close relative, the field-programmable gate array (FPGA), are both single-chip devices containing  $10^5$  or more gates that can be connected via a downloaded set of instructions to perform complex digital functions from simple Boolean processing to complex arithmetic. In our case the CPLD is used as a convenient interface between the PICNIC camera digital output and the single-board computer dedicated to fringe tracking and data acquisition.

Our CPLD is an Altera 10K70, which is mounted on a PCI-PMC card.<sup>7</sup> The single-board computers share an area of their internal memory with a SUN workstation. Through VxWorks the computers can access the SUN hard drive. An advantage of this configuration is that we can load a new circuit in the CPLD from the computer memory or from the hard drive during operation. A disadvantage of having the CPLD pre-wired to a board is that outputs are forced to be assigned to specific components and I/O pins, which prevents the Altera compiler from freely assigning these pins and from optimizing the routing of signals. Fixed output pins can thus add delays to the circuit and make it failure-prone at higher speed.

### 3.4. Clocking the Detector

For applications needing low read noise, such as infrared interferometry, a great advantage of the PICNIC and NICMOS3 detectors is that one can nondestructively read out any

desired group of pixels. At IOTA the six output signals from the beam combiner (which derive from the pairwise combination of beams from three telescopes) are separately focused on 6 pixels and read as fast as is allowed by settling times in the detector and analog-to-digital converter (ADC).

To start, the detector pixels must be “reset” by connecting them briefly to a bias potential (0.7 V). After reset, the incident photons generate photoelectrons that cause the output voltage to decrease. When the pixel bias voltage reaches zero, the array is said to be “saturated” and needs to be reset again in order to be responsive. To read out a pixel, we first select the appropriate pixel and line, then measure the voltage on the pixel and subtract from the previous sample.

### 3.5. Scan Mode Readout

In scan mode, pixels are read at requested coordinates. The time-series signal from each pixel is the interferogram, which is generated by combining the light from a telescope pair and linearly sweeping the relative delay through a path difference on the order of 50–100  $\mu\text{m}$  (see Fig. 2). There is a small but finite gain in clocking efficiency and noise if these pixels are closely spaced and located on the same line. The cycle is repeated 1–10 times per second, depending on the photon rate from the star (slower for fainter stars). Typically, each scan contains 256 data points, and an observation typically consists of 100–1000 scans. Observations alternate between the target star and a calibrator star unresolved by the interferometer (or of known angular size).

#### 3.5.1. Fowler Sampling

In scan mode, the array is reset at the start of each scan, after which the pixels of interest are sampled continuously as they discharge (Fowler & Gatley 1991). Each recorded data point is the difference between consecutive samples, and the integration time per data point is set by the time needed to sample each target pixel, possibly multiple times, as described below. Avoiding the array reset for every data point reduces the noise and increases the readout speed, although at the expense of dynamic range.

#### 3.5.2. Readout Parameters

In readout mode there are six control parameters as follows: (1)  $T_{\text{step}} = N_{\text{base}}/f$  is the time to step from one pixel to another, and  $f = 33$  MHz is the base clock speed in the CPLD; typically,  $N_{\text{base}}$  is 85 but ranges from 33 to 255. (2)  $N_{\text{skip}}$  is the number of pixels skipped between sampled pixels. (3)  $T_{\text{del}}$  is a settling time delay between the PICNIC clock and the sample assertion to the ADC, typically 4  $\mu\text{s}$ . (4)  $N_{\text{loops}}$  is the number of times that a group of pixels is read; typically 4 loops but ranging from 1 to 7. (5)  $N_{\text{reads}}$  is the number of times per visit that a pixel is read and the value summed with previous reads in that visit; typically 4 reads but ranging from 1 to 16. (6) The “readout sequence” vector contains detailed clocking instructions to access each pixel. (7)  $N_{\text{smpl}}$  is the number of samples per scan stored in memory, typically 256.

<sup>7</sup> A PCI-PMC card connects to a mechanically modified version of the PCI bus commonly used in personal computers and plugs directly on top of one of our single-board computers.

TABLE 1  
INTEGRATION TIMES

$N_{\text{loops}}$	$T_{\text{int}} (\mu\text{s})$			
	$N_{\text{reads}} = 1$	$N_{\text{reads}} = 2$	$N_{\text{reads}} = 3$	$N_{\text{reads}} = 4$
1 .....	340	510	670	830
2 .....	660	990	1320	1640
3 .....	980	1470	1960	2450
4 .....	1300	1950	2610	3270

NOTE.—Typical integration time,  $T_{\text{int}}$  ( $\mu\text{s}$ ), from eq. (1) as a function of  $N_{\text{loops}}$  and  $N_{\text{reads}}$ , for a set of six pixels at a typical location of the PICNIC detector. The table agrees with the experimental data within 6%.

Note that “sample” here means a snapshot of the set of measured pixels, where the specified number of loops and reads all contribute to a single such sample. (8)  $N_{\text{pix}}$  is the number of pixels illuminated by the output of the combiner (6 in the current implementation).

### 3.5.3. Integration Time

The integration time per scan,  $T_{\text{int}}$ , is given by

$$T_{\text{int}} = N_{\text{smp}} N_{\text{loops}} \left\{ T_{\text{step}} [N_x + (N_{\text{pix}} - 1) N_{\text{skip}} + 1] + T_{\text{read}} N_{\text{reads}} N_{\text{pix}} \right\} + N_y T_{\text{step}}. \quad (1)$$

Here  $T_{\text{read}}$  is the time to read once and digitize the voltage at a single pixel; typically this is 10  $\mu\text{s}$  plus a settle and wait time

of  $T_{\text{del}} = N_{\text{del}}/f$ , where  $N_{\text{del}}$  is in the range 85–511 (a typical value is 506), and  $N_x$  and  $N_y$  are the position of the pixel with respect to the origin. The other quantities were previously defined. As examples, we show in Table 1 the value of  $T_{\text{int}}$  for a range of typical loops and reads. These values were experimentally verified to an accuracy of 6%. Figure 2 shows interferograms obtained with this readout mode.

The PICNIC camera is faster than NICMOS3 camera, for several reasons: (1) The pixel clock in PICNIC triggers on both the rising and falling edges of the clock waveform, whereas in NICMOS3 the trigger was only single-edged. The gain is a factor of 2 in clocking along the pixel ( $x$ ) direction. (2) Clocking through the CPLD is faster than clocking using PC programmed I/O (1 vs. 0.3 MHz), giving an additional factor of 3 gain in speed. Faster clocking indirectly helps to reduce noise in a given amount of observing time, because more reads per second (see § 5.2) produces lower net noise per second.

### 3.6. Image Readout

The camera’s principal use is reading out a small number of pixels illuminated by the beam combiner, but it is also necessary to read a whole quadrant (see Fig. 3) for optical alignment purposes. Details of the implementation of this readout mode are given in Appendix B and in Pedretti (2003).

## 4. SOFTWARE

The camera software controls tasks in three areas: (1) communication between the real-time computer and the CPLD; (2)

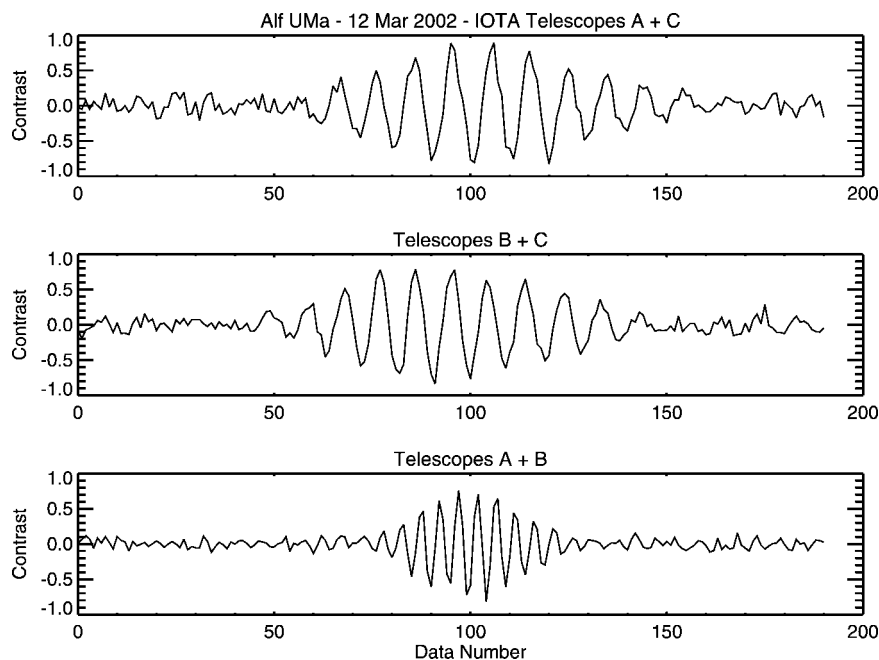


FIG. 2.—Example of  $H$ -band scans obtained using the CPLD interferogram readout circuit. These data were obtained using the IONIC-3T combiner (Berger et al. 2003). Complementary fringes for each telescope pair have been subtracted to remove common mode coupling fluctuations due to atmospheric seeing, and enhance the coherent signal. The picture consists of raw single scans and was taken from the real-time display software routinely used at the IOTA.

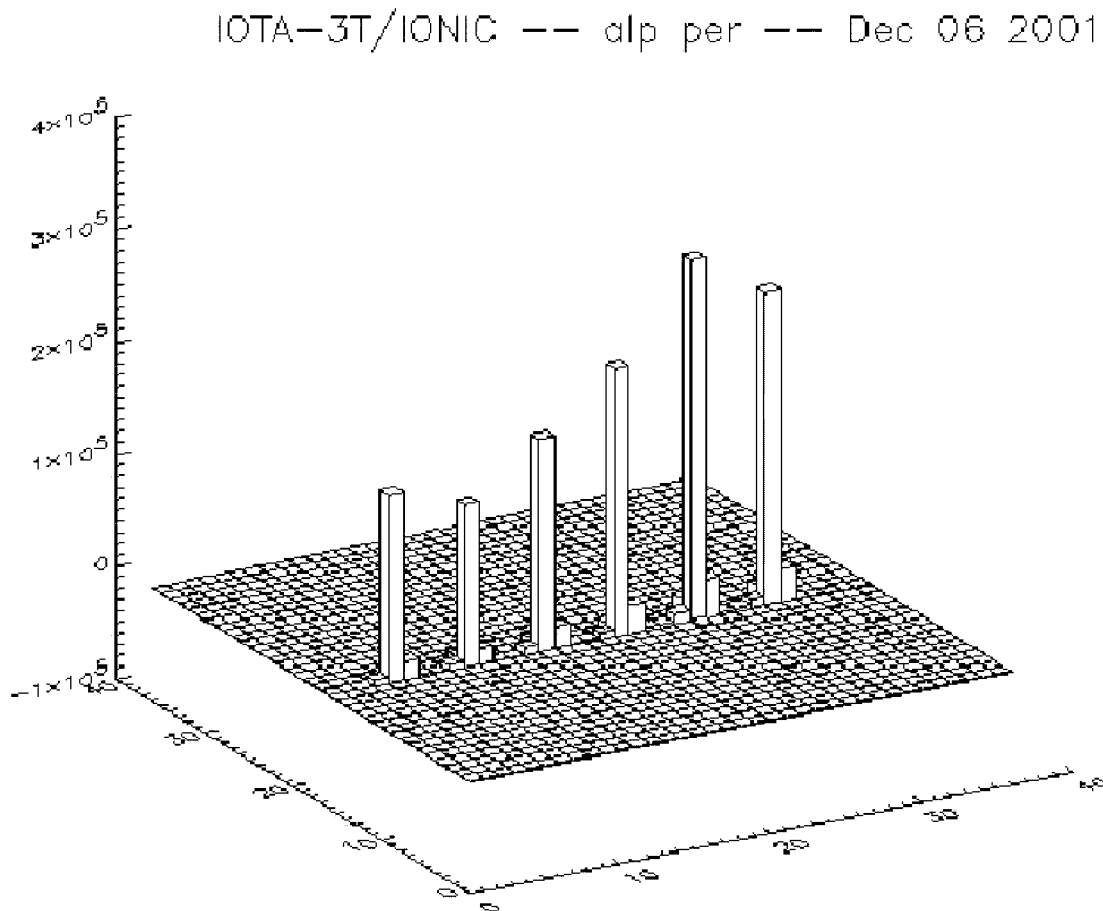


FIG. 3.—Example of a frame showing the pixels illuminated by the six outputs of the IONIC-3T beam combiner, imaged in quadrant readout mode.

visualization of the data; and (3) control of the delays for fringe tracking. The communication software (C, C++) controls the task of writing to the control register of the CPLD to modify its actions, and the task of reading the static RAM in the CPLD and transferring its contents to a data buffer for display and analysis.

The visualization software (IDL) provides a graphical interface to the user and sends commands to the real-time system. In the initial alignment mode, this software displays an image of the PICNIC quadrant or subquadrant so that the observer can see on which pixels the star images are falling and make appropriate corrections to center the images on the selected target pixels. In data-acquisition mode, this software displays the raw interferograms, as shown in Figure 2. The software also provides an interface for user selection of the parameters of the data-acquisition and fringe-tracking systems.

The fringe-tracking software (C, C++) generates the fringe-scanning motions in the delay paths and servo controls their position so that all three fringe packet pairs from the three telescopes arrive at the detector at nearly the same time. The latter function is a prerequisite for making useful phase-closure measurements at IOTA. The fringe-scanning motion is accomplished by moving an infrared reflecting dichroic driven by a piezo

transducer with a  $60 \mu\text{m}$  stroke (Physik Instruments) and commanded by a digitally generated ramp from the fringe-tracking software. After each ramp, the centroid of each pair of recorded interferograms is estimated by a novel fringe-packet-tracking algorithm, which will be described in detail elsewhere (Pedretti 2003; E. Pedretti, J. D. Monnier, & W. A. Traub, 2003, in preparation). Two other independently written fringe-packet-tracking algorithms have also been tested (Thureau et al. 2003; E. Wilson 2003, in preparation). A typical correction signal is a few microns of optical path difference after each stroke.

## 5. DETECTOR PERFORMANCE

### 5.1. Read Noise and Gain Measurements

The gain was measured using the standard Poisson-statistics method. A light source connected to an adjustable regulated DC power supply was used to provide varying degrees of illumination to the array. For each DC voltage setting, we recorded scans identically as in science fringe acquisition mode, using in this case  $N_{\text{loops}} = 1$ ,  $N_{\text{reads}} = 1$ , 6 pixels, and 128 read cycles. Two combinations of pixel-to-pixel step time ( $T_{\text{step}}$ ) and pixel sample delay ( $T_{\text{del}}$ ) were used, i.e., ( $2.5 \mu\text{s}$ ,  $15 \mu\text{s}$ ) and

TABLE 2  
READ NOISE AND CAMERA GAIN DATA

Pixel	$t_{\text{int}}$ ( $\mu\text{s}$ )	$\sigma_{\text{read}}$ ( $e$ )	$g$ ( $e \text{ ADU}^{-1}$ )
0	310	$10.81 \pm 0.26$	$2.43 \pm 0.05$
1	310	$8.82 \pm 0.17$	$2.22 \pm 0.03$
2	310	$16.15 \pm 0.27$	$2.40 \pm 0.04$
3	310	$14.62 \pm 0.25$	$2.46 \pm 0.04$
4	310	$16.21 \pm 0.24$	$2.22 \pm 0.04$
5	310	$13.09 \pm 0.24$	$2.42 \pm 0.04$
0	130	$8.74 \pm 0.36$	$2.36 \pm 0.08$
1	130	$8.04 \pm 0.37$	$2.17 \pm 0.07$
2	130	$12.93 \pm 0.45$	$2.36 \pm 0.08$
3	130	$12.25 \pm 0.43$	$2.38 \pm 0.08$
4	130	$12.98 \pm 0.54$	$2.31 \pm 0.09$
5	130	$13.58 \pm 0.40$	$2.34 \pm 0.07$

NOTE.—Numerical results of the read noise  $\sigma_{\text{read}}$  and camera gain  $g$  measurements (see Fig. 4). The noise is given per double read, given the differencing of consecutive samples intrinsic to our sampling method. Averaging over both integration times  $T_{\text{int}}$ , the average read noise is  $\sigma_{\text{read}} = 12.4 \pm 0.8 e$ , and the average gain is  $g = 2.34 \pm 0.03 e \text{ ADU}^{-1}$ .

( $1.0 \mu\text{s}$ ,  $4 \mu\text{s}$ ). The corresponding integration times are 310 and  $130 \mu\text{s pixel}^{-1}$ , respectively. The  $310 \mu\text{s}$  value was selected to be representative of a relatively slow readout, while the  $130 \mu\text{s}$  value is the fastest readout speed that we have used, based on recommendations by Rockwell and experimentally verified monitoring of the detector output with an oscilloscope. The measured mean (ADU) and variance  $\sigma^2$  (ADU $^2$ ) for each pixel are plotted in Figure 4.

We assume that the photoelectron noise from the incident light has Poisson statistics. The gain  $g$  ( $e \text{ ADU}^{-1}$ ) is then the inverse of the slope of the variance versus mean curve. The read noise is derived from the variance intercept at zero mean. The results of these 12 experiments are shown in Table 2.

### 5.1.1. Gain

A number of conclusions follow from Table 2. (1) The gain values are nominally independent of pixel position, with a mean value of  $g = 2.34 \pm 0.03 e \text{ ADU}^{-1}$ , where the uncertainty is the mean error. (2) The gain does not change significantly when the clocking speeds are changed, as might be expected. (3) The

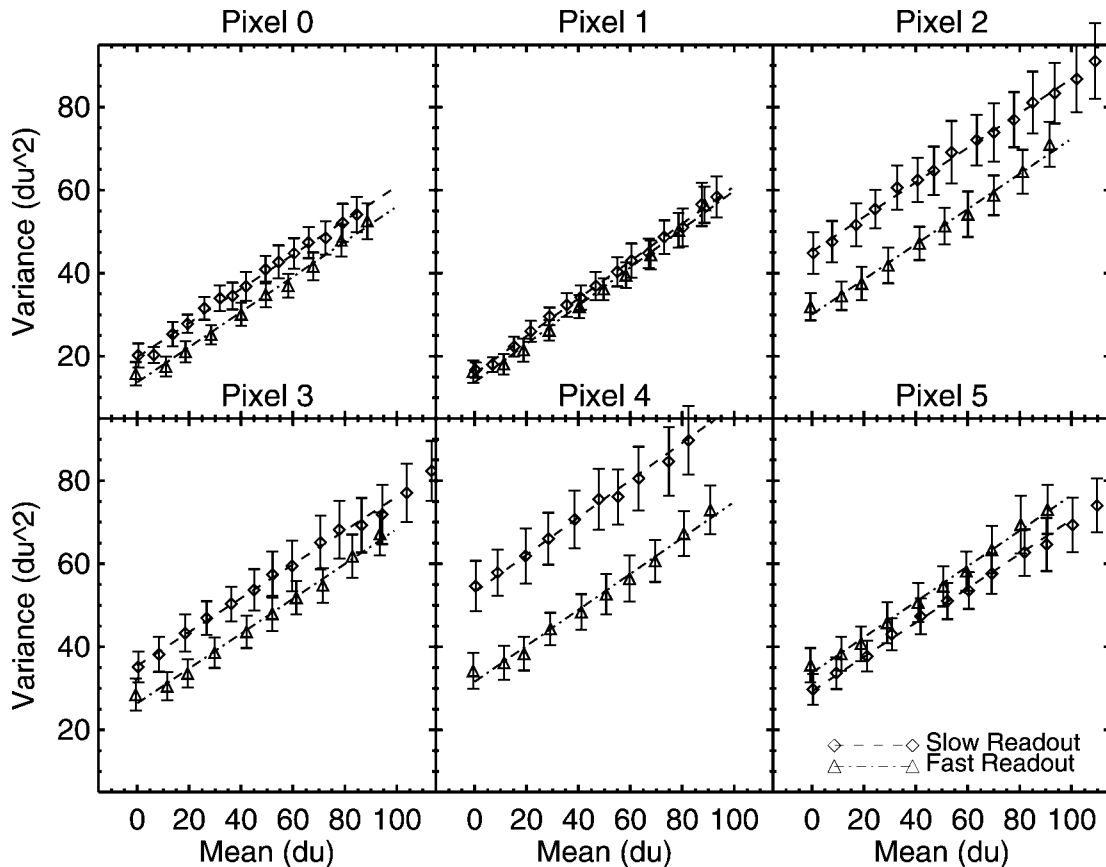


FIG. 4.—Variance vs. mean plot to measure system parameters. Data are plotted for six pixels sampled in interferogram mode. The two data sets in each plot were obtained for: (a) a slow readout mode (390 KHz PICNIC clock speed and  $15 \mu\text{s pixel}^{-1}$  sampling delay) and (b) fast readout (1 MHz clock speed and  $4 \mu\text{s pixel}^{-1}$  sampling delay). In each case, the slope provides the camera gain ( $e \text{ ADU}^{-1}$ ), and the y-axis intercept provides the read noise; the resulting gain and read noise values are listed in Table 2.

gain values appear to vary slightly from pixel to pixel, with an rms scatter of 4%.

### 5.1.2. Read Noise

The corresponding conclusions on read noise are as follows: (1) The read noise has a mean value of  $\sigma_{\text{read}} = 12.4 \pm 0.8 e$ , where the uncertainty is the mean error; the  $\sigma_{\text{read}}$  value refers to the rms variation in the difference of two successive reads, so the single-read rms value may be inferred to be smaller by  $\sqrt{2}$ , giving  $\sigma_{\text{single-read}} = 8.8 \pm 0.6 e$ . (2) The read noise is slightly higher for the longer integration time samples, i.e.,  $13.3 \pm 1.1 e$  for 310  $\mu\text{s}$  integration, compared to  $11.4 \pm 0.9 e$  for 130  $\mu\text{s}$ . More experiments need to be done to see if this effect is real and what its cause might be. (3) The read noise varies significantly from pixel to pixel, with an rms scatter of 22%. This suggests that it is profitable to select an optimal set of pixels for science operation, although in the present work no attempt was made to select particular pixels.

It is instructive to compare this performance with that of our previous NICMOS3 system (Millan-Gabet et al. 1999). We note that the electronics design is basically the same for both systems, but the readout systems are physically distinct (i.e., we use separate electronics). Millan-Gabet et al. (1999) quotes a read noise of 24.6  $e$  per difference of two successive reads in the readout mode normally used for fringe detection (i.e., using loops and reads to access the two output pixels). The corresponding read noise for the present PICNIC system, as discussed above, is 12.4  $e$  per difference of two successive reads in normal fringe-readout mode in which loops and reads are used to access (in this case) six pixels. *Thus the PICNIC system has a smaller read noise by a factor of 2.0.* This improvement is likely due to the chip itself, as well as improvements in our electronics, but since the chips are clocked differently, we could not use the same electronics for both chips, and therefore we cannot determine what part of the improvement is due to the chip itself and what part is owed to the electronics.

### 5.2. Noise Reduction with Multiple Reads

We measured the reduction of read noise with multiple read averaging. We recorded 128 sample data sets, with no illumination on the detector under various readout modes, and with 1 to 16 reads per sample. Dark current, as well as a background light leakage, would contribute extra counts and associated variance to the data with longer integration times, so to remove this effect we computed the mean (in electron units) of each scan and subtracted this value from the variance (also in electron units). The remaining amount of variance is then attributable only to the action of reading each pixel, and the square root of this value is the rms read noise. In Figure 5 we show these rms read noise values as a function of the number of averaged reads. Data for both the slow (310  $\mu\text{s}$ ) and fast (130  $\mu\text{s}$ ) readouts are shown, and both give similar results. For each data set, the ideal response with slope of  $-\frac{1}{2}$  is shown (the slope expected if the

rms read noise were to decrease as the inverse square root of the number of reads). The data shows that this technique works well up to at least 16 reads. Therefore, to improve the quality of an astronomical observation, it is always best to make as many reads as possible consistent with other constraints such as the atmospheric coherence time (for poor seeing conditions) and the saturation time of the detector (for bright stars). The result for our PICNIC detector is in agreement with that previously found for our NICMOS3 detector (Millan-Gabet et al. 1999).

### 5.3. Magnitude Limit

Although the present paper is devoted to the PICNIC camera and electronics, it is nevertheless worthwhile to briefly mention how the camera performs at the IOTA interferometer. In Millan-Gabet et al. (1999) we demonstrated that the IOTA was able to make useful measurements at  $H$  band on a star with  $H = 7.2$ , which was approximately the limiting magnitude of the interferometer for a point source. The system components at that time were the IOTA two telescope interferometer, a free-space beam combiner (i.e., no single-mode fibers), and the NICMOS3 camera.

Recently we made a comparable quality measurement of simultaneous interferograms in  $H$ -band on a star with  $H = 7.0$ , which is very similar to our previous magnitude limit. The system components in this case were the IOTA three telescope interferometer, the IONIC-3T beam combiner (using single-mode input fibers as in Berger et al. 2003), and the PICNIC camera described in the present paper.

Several gain and loss factors enter into a comparison of limiting magnitudes in the two cases, as follows. Regarding losses, the new system has only one-half the amount of light per detector pixel compared to the old system, owing to the extra split required in order to combine the light from a given telescope with that of two (instead of one) other telescopes. Another potential loss occurs with the new system because we are focusing the star onto a single-mode fiber of core diameter 7  $\mu\text{m}$  instead of a 40  $\mu\text{m}^2$  detector pixel, and the theoretical coupling factor into the fiber is 75%. Yet another loss occurs from the finite transmittance of the integrated optics (IONIC-3T) beam combiner, which in the lab has a measured throughput of about 0.6 (J.-P. Berger 2002, private communication).

Regarding gains, the new system has a measured noise level that is lower than in the old system by a factor of about 2.0 (see § 5.1.2). Also, the new system can be clocked faster (see § 3.5.3), so we can make up to about 6 times more reads per unit time, and therefore achieve up to a factor of 2.4 lower noise. In addition, in the new system we replaced the aging coatings on the siderostats and secondary mirrors of the two original telescopes for an unknown gain, perhaps a factor of 1.5.

On balance, we see that the potential loss factor is roughly 0.2, but the gain factor is roughly 7, for a net gain factor of 1.4, although this value is relatively uncertain. In fact, we did achieve a slightly fainter limiting magnitude with the new sys-

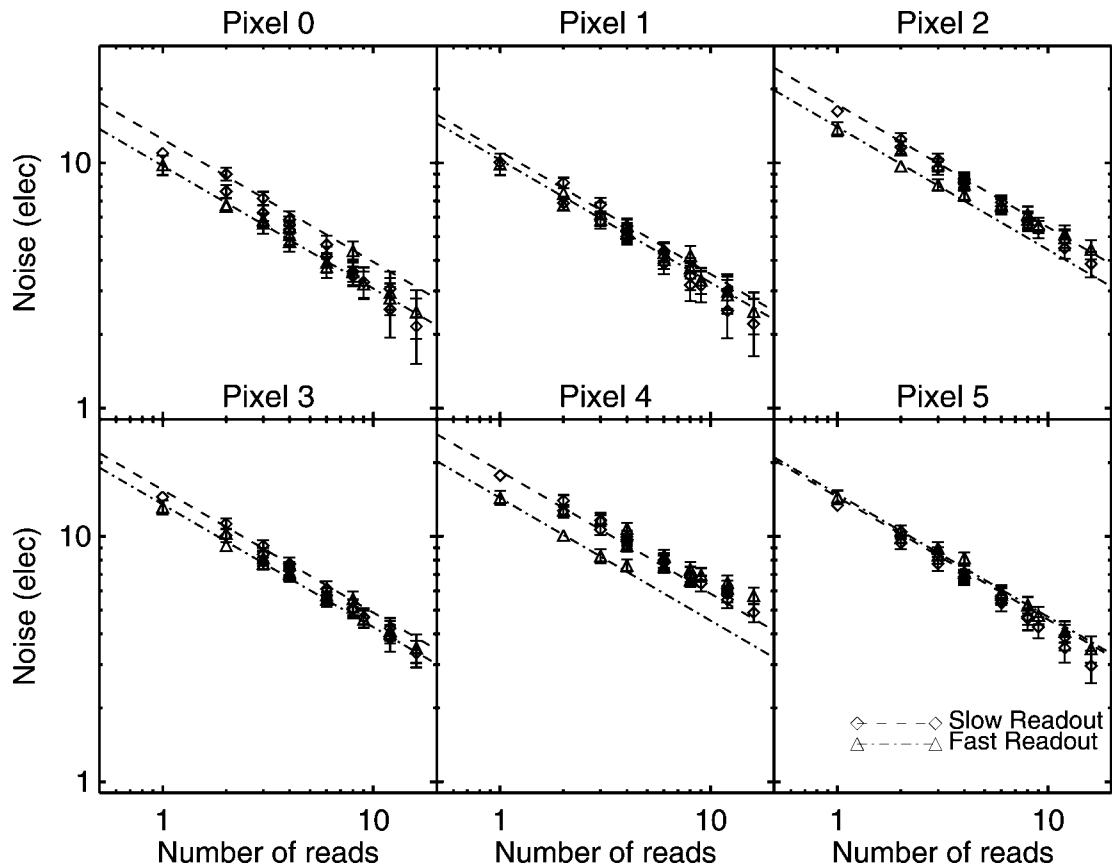


FIG. 5.—PICNIC camera measurements of noise vs. number of reads under zero illumination for six pixels read in interferogram mode. As can be seen, noise reduction follows closely the ideal relation ( $\text{noise} \approx 1/\text{reads}^{1/2}$ ), plotted in dashed lines. Using this technique, we measured a lowest read noise value of  $2.2 \pm 1 e$  for the best pixel.

tem, so in a rough sense we have validated the gain calculations. More importantly, the value of this gain/loss calculation is that it points out areas where we might achieve yet further gains for even fainter limiting magnitudes.

## 5.4. Nonstandard Behaviors of Camera

### 5.4.1. CPLD Spikes

We observed that our data had frequent and strong spikes superposed on it when the room air temperature near the CPLD was greater than about  $70^\circ\text{F}$  ( $21^\circ\text{C}$ ). The spikes were generated by digital errors in the CPLD, and their frequency of occurrence increased monotonically with temperature above this critical value. At worst, there was a spike every few data points. The temperature of the CPLD itself was well above room temperature, since it was mounted on top of the CPU of a single-board computer and was in a card cage slot next to another CPU. The solution is simply to keep the room relatively cool, below  $70^\circ\text{F}$ .

### 5.4.2. Settling Time after Reset

After a frame reset, we found that the pixel signal was not usable for a period of about 50 ms. During this time the voltage output looked approximately like a capacitor charging curve, with a superposed oscillation of smaller amplitude. After this time, the pixel voltage followed the expected linear behavior. A similar effect was also observed in our NICMOS3 camera, but with a much shorter timescale of about 8 ms. Given the experience of other groups with PICNIC arrays, it appears unlikely that this long transient after reset is an intrinsic property of the detector; however, a root cause in our electronics or readout method has not yet been identified.

### 5.4.3. Pixel Interaction

We have observed that when a single pixel in the row containing the interferometric signals is strongly illuminated (but not saturated), the dark level on neighboring pixels are corrupted: the photometric signal becomes negative, clearly an effect due to an analog transient and not a true light or charge leakage effect. This situation occurs naturally and frequently

in our observational sequence, as the beams from the three telescopes are sequentially shuttered in order to measure the transmission coefficients of our beam combiner, and therefore poses a potential significant limitation to the calibration of the fringe signals.

Although all pixels in a quadrant share the same on-chip output and amplifier electronics, our sampling rate is inside the 100 KHz bandwidth of our analog chain, so insufficient bandwidth could not produce such an effect by not being able to follow large output voltage swings associated with large pixel-to-pixel differences in signal. We also see that the electronics chain has no trouble following the large and sharp voltage swings associated with disconnecting the output as part of the  $N_{\text{loops}}$  averaging. Therefore, we currently have no good explanation, and this effect is being investigated further.

#### 5.4.4. Effect of Pixel Saturation

We focused a bright star on a target pixel and noted that the resulting signal was nearly constant in time, as expected, until the pixel well was depleted; after depletion the signal was essentially zero, again as expected. (In our case the full well was about 145,000  $e$ .) However, when we sampled the adjacent pixel in the same line, we saw an opposite behavior, with a small constant signal prior to saturation of the target followed by an increased constant signal after saturation. The magnitude of the increase was roughly 15% of the target signal. We did not explore this behavior thoroughly, but in the cases we did examine, it appeared to be robustly repeatable.

## 6. CONCLUSION

We describe a new CPLD-controlled infrared camera for the IOTA interferometer. The CPLD architecture allows on-the-fly reconfiguration of the readout circuit to achieve different functions on the same hardware. Typical readout modes include full quadrant, subarray of quadrant, single pixel, and a set of preselected pixels. All of these modes have a wide range of timing options. This architecture allows fast and stable clocking of the PICNIC array, resulting in faster and lower noise readout.

In fringe detection mode, the measured rms readout noise for a single read of the detector is  $\sigma_{\text{single-read}} = 8.8 \pm 0.6 e$ . In

normal readout mode the difference of two successive reads is larger by  $\sqrt{2}$ , giving  $\sigma_{\text{read}} = 12.4 \pm 0.8 e$ . With  $M$  multiple reads of a given pixel, the read noise averages down as  $\sigma_M = \sigma_{\text{read}}/\sqrt{M}$  for at least the range  $1 \leq M \leq 16$ , showing that fast, multiple reads significantly improve performance in the PICNIC detector. Coupled to the recently installed IONIC-3T integrated-optics three-beam combiner at IOTA, we have successfully measured triple interferograms on stars as faint as  $H \approx 7$ . With this level of sensitivity, IOTA can extend its two-telescope programs on evolved stars and young stellar objects to closure-phase measurement and imaging mode.

The CPLD-based architecture demonstrated here is ideally suited for the current state of the optical/infrared interferometry field. A variety of test beds are exploring various beam combination techniques that need different readout modes to be implemented at high speeds and stability. Cutting-edge detectors are used, and it is often necessary to design the readout electronics from scratch. CPLDs are fast-track technology that allow the creation of a uniform interface to data-acquisition software that can keep pace with the rapidly evolving hardware of the new powerful imaging arrays now coming on line.

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## APPENDIX A

### CIRCUIT DEVELOPMENT PROCESS WITH CPLDs

The Altera device used in this project (EPF10K70) is routinely used for the visible star-tracker camera and the PICNIC science camera. In more than 2 years of operation, these components have been reprogrammed several times during each observation, without failure and with perfect repeatability.

In order to develop our digital project, we used the Altera

MAX+PLUS-2 design software, which supports schematic as well as VHDL<sup>8</sup> and AHDL<sup>9</sup> entry. We experimented with all the above methods and determined to use a combination. It

<sup>8</sup> Acronym of VHSIC hardware description language, where VHSIC is for "very high speed integrated circuit."

<sup>9</sup> Acronym of Altera hardware description language.

seems faster to develop complex nonstandard logic functions and the state machines in VHDL or AHDL and then interconnect the blocks using schematics entry. We generally prefer to use VHDL rather than AHDL, because VHDL is an industrial standard, but online help for the AHDL compiler is far better than that for the VHDL. These compilers were made freely available to us through the Altera University Program.

A big limitation of these development tools, we found out, is in the simulator; a circuit working in simulation is not guaranteed to work once it is transferred to the real hardware. The Altera simulator seems to be somewhat inferior to other

commercially available simulators, probably because the circuit is so easily reprogrammable. For this reason we resorted to using the simulator for eliminating gross digital design errors and tuned the circuit on the hardware itself.

Another problem found was that a slight modification to the circuit (like adding a test point to sense an internal signal) could cause malfunctioning in other areas of the circuit that were totally independent from the modified area. This would suggest that the compiler can dramatically change the routing of the internal signal for every added modification, changing then all the internal delays.

## APPENDIX B IMPLEMENTATION OF THE QUADRANT READOUT MODE

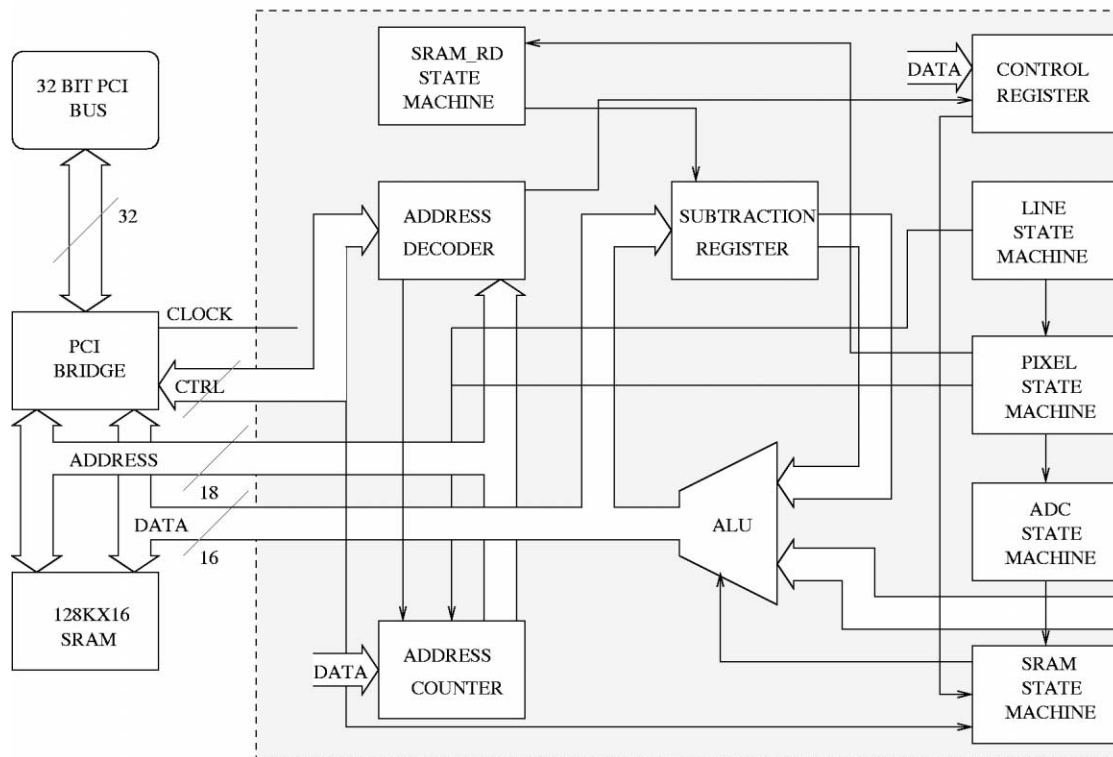


FIG. 6.—PICNIC quadrant readout circuit. Five state machines are responsible for the operations of the camera. Complex functions are broken into elementary functions of clocking lines, pixels, resetting the detector, commanding the ADC and transferring data into SRAM, each executed by a single-state machine.

Although the camera's principal use is reading out a small number of pixels illuminated by the beam combiner, it is necessary to read a whole quadrant for optical alignment purposes. Moreover, in this mode the camera could be used as an IR wavefront tip-tilt sensor to track sources that are too faint at visible wavelengths to be observed using our current CCD-based system. A block diagram of the CPLD circuit in quadrant mode is shown in Figure 6.

### B1. CORRELATED DOUBLE SAMPLING

In correlated double sampling (CDS) mode, adopted for quadrant readout, the detector is reset, sampled (reset frame), allowed to integrate and resampled (image frame). The difference between the reset and image frames is then recorded. This is the basic operational mode of the NICMOS3 and PICNIC detectors, both of which are integrating detectors with non-

destructive readout. CDS is implemented entirely in the CPLD electronics. The CPU receives a buffer containing the final, ready-to-use data. Unless otherwise stated, in this paper we use the term “read” to mean a CDS read cycle.

## B2. CIRCUIT IMPLEMENTATION

The quadrant-image read is stored in the static RAM (SRAM) on the Technobox PCI-PMC card, which is shared between the CPU and the CPLD through the PCI bus. The readout starts when the start bit in the control register of the CPLD is asserted by the CPU. The interrupt line (INTA) is asserted when the readout process has finished and a frame is present in the SRAM.

Between these events, many operations are handled in parallel by state machines that have been built into the CPLD. These state machines are as follows:

1. *SRAM state machine*.—Handles communications with the PCI bridge for bus arbitration. It polls the start bit of the control register and sets a semaphore that starts the LINE state machine. When a reset frame and an image frame have been acquired and subtracted, it releases the PCI bus and asserts INTA.

2. *LINE state machine*.—Controls the FSYNC and LINE clock generation for the PICNIC array. Once a line has been selected, it sets a semaphore to start the PIXEL clock generation; lines are counted by the line counter. It will also assert the RESET line together with LSYNC if the toggle flip-flop, which keeps the state of the frame (reset frame or data frame), is set on reset frame.

3. *PIXEL state machine*.—Controls the LSYNC and PIXEL clock generation for the PICNIC array. It controls the sequence of clocks and sets a semaphore when the ADC can sample the selected pixel; pixels are counted by the pixel counter.

4. *ADC state machine*.—Controls the ADC. If the toggle flip-flop is in reset frame state, then the ADC state machine sends a start-of-conversion pulse to the ADC, waits for the end-of-conversion signal from the ADC, and writes a word of data in the static RAM. If the toggle flip-flop is in data-frame state, then the ADC state machine stores the difference between the data word at the current SRAM address and the data word

obtained from the ADC. The SRAM address is obtained by combining the line counter and pixel counter.

5. *READ-SRAM state machine*.—Reads one word of the reset frame previously written to SRAM, during the ADC conversion. This operation is carried out in parallel with the ADC data conversion. The data previously stored in memory and addressed by the ADC state machine is recovered and stored in a temporary register. This value will be used to calculate the difference between the reset value and the current value obtained from the ADC converter.

The data acquisition (DAQ) scheduler task, running on the CPU when in quadrant mode, loads the circuit into the CPLD and initializes the readout parameters. The start bit is then asserted in the CPLD control register, the state machines are started, and the controller runs in a loop until a whole quadrant is acquired.

## B3. READOUT PARAMETERS

A number of readout parameters can be changed by the application running on the CPU by accessing the registers on Altera. The registers are as follows:

1. Tstep is the pixel-to-pixel step time. The 33 MHz PCI clock is divided by a programmable counter built into the CPLD in order to generate the base clock rate used to clock the PICNIC array; the counter can be programmed by the CPU through the PCI bridge. A typical value is 1  $\mu$ s.

2. Tdel is the delay between the PICNIC clock and the sample assertion to the ADC. This delay is necessary to avoid sampling the addressed PICNIC pixel before it has settled. The delay is generated by a programmable counter and is accessible to the CPU through the PCI bridge. A typical value is 4  $\mu$ s.

3. Tintdel is the time between the reset frame and the image frame implemented with a presettable counter. A typical value is a few ms.

4. (Nx, Ny) is the subquadrant corner position in units of pixels (see § 3.5.3). With these variables it is possible to define a small area of the detector. This flexibility will be crucial when implementing an IR wavefront tip-tilt sensor.

## APPENDIX C

### IMPLEMENTATION OF INTERFEROGRAM DETECTION MODE

This mode reads a number of pixels located at arbitrary coordinates on the PICNIC array for detection of interference fringes. In practice, for better clocking efficiency and noise performance, the pixels should be closely spaced and, preferably, on the same line. A block diagram of the CPLD circuit in interferogram detection mode (also called scan mode) is shown in Figure 7.

#### C1. CIRCUIT IMPLEMENTATION

The digitized pixel voltages are stored in SRAM. INTA is asserted at the end of every group of pixels that are read out. INTA is used to delimit the end of a data frame, but it is also used to step the piezo OPD scanner, which is synchronous with data acquisition. This simple cycle is executed once per data



TABLE 3  
CPLD MICROCODED INSTRUCTIONS

Instruction	Hex Value	Action
fsync .....	02	FSYNC pulse generated
lsync .....	03	LSYNC pulse generated
line .....	00	LINE clock transition $n$ times PIXEL clock transition $n$
pixel .....	01	times
jump .....	04	Jump to program location

NOTE.—CPLD microcoded instructions used to generate scanning sequences in interferogram readout mode.

reads is greater than 1, then the state machine reads the ADC several times, and the values are accumulated in the corresponding pixel register.

5. *sram\_wr\_process state machine*.—Executes the data transfer to SRAM from the internal registers when the requested loops and reads are completed. When the sequence starts again to sample a new data point, it executes in parallel, transfers the data from the pixel registers to SRAM, and sends an interrupt when the process is completed.

## C2. MICROCODED INSTRUCTIONS

It is highly desirable to have the flexibility of choosing which pixels are sampled in order to use different combiners. For this reason the scanning sequence has to be alterable. This was solved by allowing the state machines to change state according to a program written into a RAM internal to the CPLD. Five

TABLE 4  
ARBITRARY CLOCKING SEQUENCE

Addr.	Hex Value	Mnemonic
0: .....	203;	- fsync+line 3
1: .....	302;	- lsync+pixel 2
2: .....	103;	- pixel 3
3: .....	004;	- line 4
4: .....	302;	- lsync+pixel 2
5: .....	103;	- pixel 3
6: .....	400;	- jump 00

NOTE.—Arbitrary clocking sequence written using the instruction described in Table 3. The first instruction (address “0”) resets the line register and clocks three lines down. The second instruction resets the pixel register and clocks 2 pixels to the right. The third instruction clocks other 3 pixels to the right. Then the detector is clocked down of other four lines and at address “4” the pixel register is reset and the pixel clocked two positions to the right. Then the pixel is clocked other three positions to the right and at address “6” the program jumps back at instruction “0” to restart the whole cycle again.

instructions can be executed by the state machines, as shown in Table 3. These instructions generate a clock sequence; the LINE clock will change level  $n$  times, according to the value of the following byte in the program. The same happens with the PIXEL clock, but in this case every pixel is read  $n$  times, according to the value written in the  $N_{\text{reads}}$  register. Loops are achieved through the jump instruction, which permits branching back to a specific instruction in the program. The loop is executed  $n$  times, according to the content of register  $N_{\text{loops}}$ . Arbitrary code for generating a clocking sequence is given in Table 4.

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